Pulse Characterization of Trapping and Thermal Effects of Microwave GaN Power FETs

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Abstract — **An experimental characterization of GaN FETs is given in this paper. A pulsed I-V pulsed S-parameters measurement set-up is used to investigate the trapping and thermal behavior of GaN MESFETs. It is shown that electrical performances are strongly affected by surface and substrate traps and that those effects are closely linked to the temperature of the device. RF measurements up to a drain voltage of 100Volts and a temperature of 320°C are presented.**

I. INTRODUCTION

Availability of high power, high efficiency microwave amplifiers is an always-growing requirement for future microwave systems. Among various III-V and I-V materials Gallium Nitride (GaN) and Silicon Carbide (SiC) appear to be the most promising ones [1]. Many works are dedicated to the development of new FET devices based on GaN grown either on Sapphire or SiC substrate, the latter providing much more efficient thermal properties. Very impressive results have already been obtained that demonstrate the strong potentialities of GaN devices [2].

However material fabrication is still in a primitive phase and thus materials suffer from serious drawbacks caused by trapping effects[3]. Moreover the power levels foreseen for the application of Nitride technology require a careful study of thermal effects.

The aim of this work is to propose a methodology based on pulsed measurements that allows investigating all the limiting factors of such devices. Moreover I-V and [S] parameters measurements can be performed in high voltage (VDS = 100V)-high current regions as well as for high temperatures (T> 320°C) using such a technique. Measurements performed in this work have shown that the trapping effects are of tremendous importance in GaN devices and that they can severely impact the electrical characteristics. Moreover it is shown that process time constants play a crucial role and that they are very sensitive to light or temperature. Finally data taken at high temperature and high voltage demonstrate the ability of GaN devices to work in such regimes.

II. MEASUREMENT TECHNIQUE

Pulsed measurement techniques have proved to give deep insight in the intimate working of power devices[4]. Applying short pulses from a quiescent bias point allows to characterize thermal effects as well as the various kinds of traps. Thus measurement sequences must be chosen in order to identify surface or substrate traps [5]. Indeed surface traps are mainly sensitive to the gate bias point [6] while substrate traps can be identified using various quiescent drain voltages for the drain. An important point concerns the time constants associated to the electron and capture process [7]. Those time constants are deeply influenced by the activation energy brought to the material either by photons or by temperature.

Indeed, considering the sequence of drain pulses represented in fig-1-a it is evident that the dissymetry in capture and emission time constants determines the number of ionized traps and consequently the drain current level.

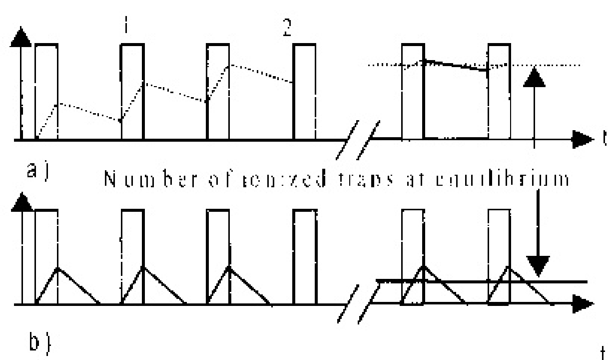

Fig. 1. Sequence of pulse measurements in with the light off a) and on b). Numbers indicate the rank of I-V measurements taken. The number of ionized traps at equilibrium strongly depend on the capture (pulse on) and emission (pulse off) time constants.

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During each positive drain voltage pulse a small quantity of traps are ionized because of the capture of electrons in the substrate or the buffer. The number of ionized traps is a function of capture time-constants and of pulse duration. When some energy is provided to the device by turning the light on for example, the emission process is activated and the time constant associated with this process is decreased as shown in fig-2-b. Thus the average number of traps decreases also and the measured current increases. This phenomenon is illustrated in fig-2.

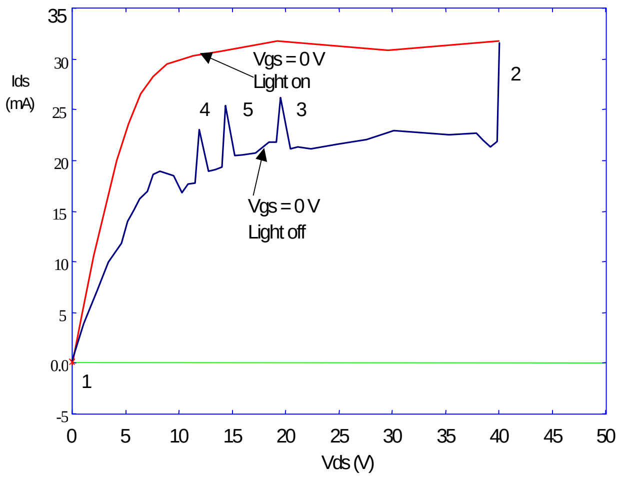

Fig. 2. Drain current measured in pulsed conditions with the light on and the light Off for a GaN MESFET with two fingers of 250µm each.

The shape of these curves deserves some explanation. When the light is turned off, the sequence of measurement points is indicated with the number shown in the figure. At first the point at VDS = 0V is measured, then the points corresponding to VDS = 40V, 20V, 10, 15V, …are successively measured, following a dichotomy measurement algorithm. Due to the very long capture time constant (several seconds), traps have no time to get filled during the first measurements and the number of filled traps get more and more important as the measurement process goes on. Thus the current measured decreases to reach equilibrium during the last measurements which correspond the part of the curve ranging from 20V to 40V. When the light is turned on this phenomenon disappears because of the strong decrease of the emission time constant. Indeed in this case equilibrium is reached very quickly and the measured curve exhibits a smooth behavior as seen on the fig-2. Moreover as the average number of ionized traps is much lower the value of the current is higher.

III- INFLUENCE OF GATE AND DRAIN QUIESCENT BIAS POINT.

As it has been shown in the previous section traps play a significant role in the shape of drain output characteristics. Further investigations will provide an insight in the two mechanisms that lead to current collapse. Those mechanisms can be identified through the pulsed measurement by varying the drain or the gate quiescent bias point.

A. Influence of Drain quiescent bias point

Buffer or substrate traps are very sensitive to drain quiescent voltage. Indeed, as the quiescent drain voltage increases more and more electrons are injected in the buffer where they can be trapped. This results in a build-up of a space charge at the interface between the channel and the buffer (substrate). This negative space charge is compensated by a positive one which reduces the channel section and consequently the drain current [7]. This is the phenomenon observed for the characteristics represented at fig-3, where a current collapse is observed when the quiescent drain voltage is increased. Moreover it can be noticed that for high pulsed voltage all the characteristics converge towards the same value. This indicates that for values of the pulse voltage higher than the quiescent value, the number of filled traps is determined mostly by the peak drain value and not by the average value as can be observed in fig-1-a.

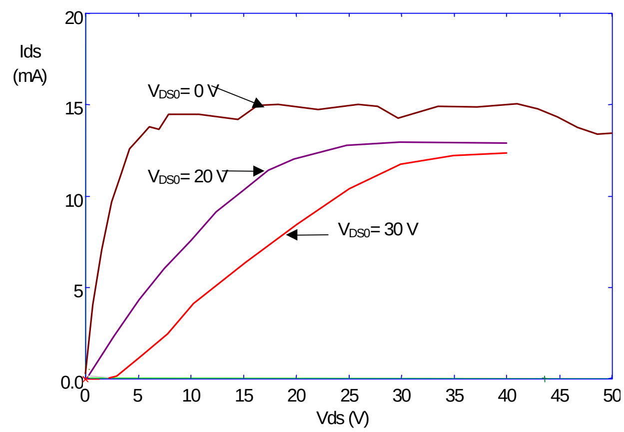

Fig. 3. Drain current of a 2x150µm GaN MESFET as a function of drain quiescent bias state (Light off). VDS0 is the quiescent drain voltage. Those characteristics were measured with a constant quiescent gate voltage VGS0=-3V

B. Influence of quiescent gate voltage

The same experiment has been performed with a fixed quiescent drain voltage

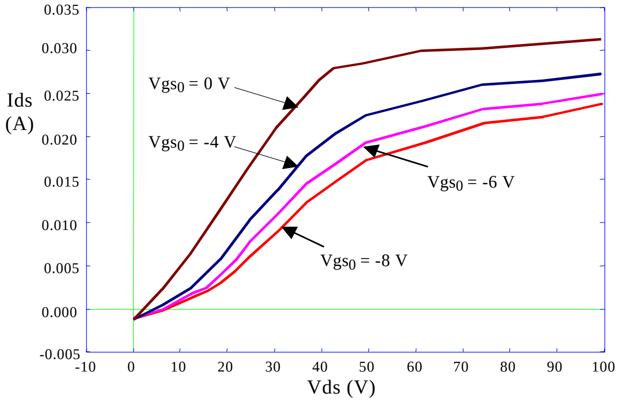

Fig-4: Influence of the quiescent gate voltage on the output characteristics. (MESFET 2x250µm).

The characteristics shown in fig-4 clearly demonstrate the presence of surface state as the drain current is reduced during the pulse when the transistor is pinched off during the quiescent state [6]

IV. MICROWAVE BEHAVIOR

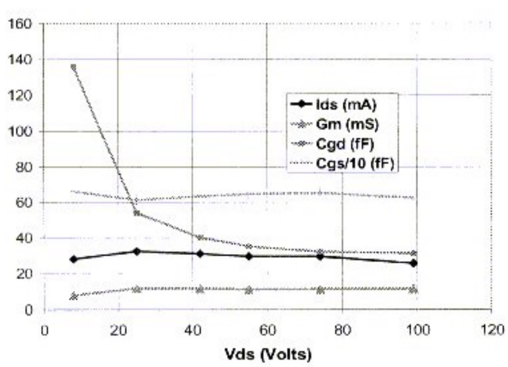

Fig. 5. Values of the intrinsic elements of the 2x250µm GaN MESFET.

Pulsed I-V pulsed S-parameters measurements allow to obtain the microwave performances of the device in the whole working range. Thus S-parameters measurements have been performed for drain voltages up to 100V in pulsed conditions. An electrical small signal equivalent circuit has been extracted for each bias point to investigate the microwave behavior of the transistor. After a de-embedding of extrinsic parameters: access inductances and resistances, the main non-linear elements of the equivalent circuit have been obtained for the following quiescent bias point: VGS0 = -3Volts; VDS0 = 0 Volt. They are represented in fig-5.

As can be seen from this figure the values of IDS, Gm, and Cgs remain roughly constant versus VDS. However the value of CGD decreases strongly as the drain pulsed voltage increases. This leads to an increase of the gain at 2GHz and of the maximum operating frequency as shown in fig-6.

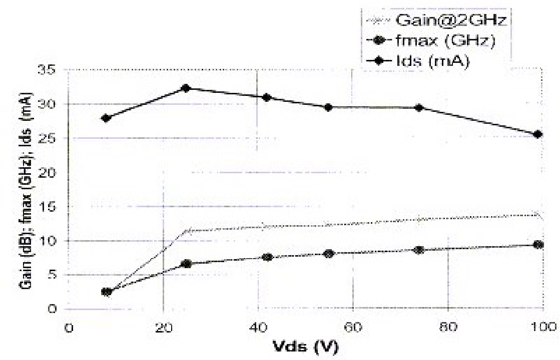

Fig. 6. Extracted Gain @ 2GHz, maximum operating frequency and current versus pulsed drain current. Quiescent gate and drain voltages are VGS0 = 0V and VDS0=0V.

It has been noted that a strong reduction of the gain is observed when traps are filled. This reduction is sought to be due to the increase of the access resistances. Indeed in the channel under the gate-drain region has a reduced section thus increasing the access resistance.

IV. THERMAL BEHAVIOR

A. Influence of the temperature on the trapping state

As it has been shown in previous sections that light has a significant influence on the value of drain current. The temperature channel is also a parameter of prime importance. To investigate the thermal behavior of the GaN MESFET, thermal measurements have been performed using on wafer pulsed measurements with a thermal chuck. Two kinds of measurements are shown in fig-7 and fig-8 with the light respectively OFF and ON.

In fig-7, when the light is turned OFF and with a quiescent drain voltage of 40V a strong increase of the drain current is observed. This increase is due to the reduction of the emission time constant with the contribution of thermal energy.

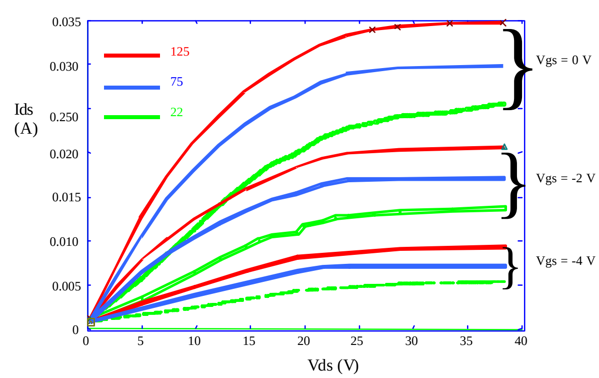

Fig-7. I-V characteristics of the 2x250µm MESFET for various temperatures.

Wide bandgap materials have the potentiality to work at high temperature. In order to test the temperature behavior of GaN devices pulsed measurements have been performed using a thermal chuck which temperature can be varied from ambient to 200°C. Higher temperatures can be reached by superimposing a DC bias point to the pulses. Thus the channel temperature can be obtained using the following relation

TChannel = TChuck + Rth VDS0 IDS0 (1)

Where *RTh* is the thermal resistance of the device. In order to determine this thermal resistance a 3D simulation of the structure has been performed. Thermal resistances obtained for 2x150µm et 2x250µm were respectively.

Wg = 150 µm, Rth = **248°C**/W,
Wg = 250 µm, Rth = **170°C**/W.

Using this technique a DC bias of 40V, 17mA has been applied to a 2x250µm device corresponding to a channel temperature of 320°C . Characteristics measured are reported on the fig-8 where no decrease of the drain current is observed even at very high temperature.

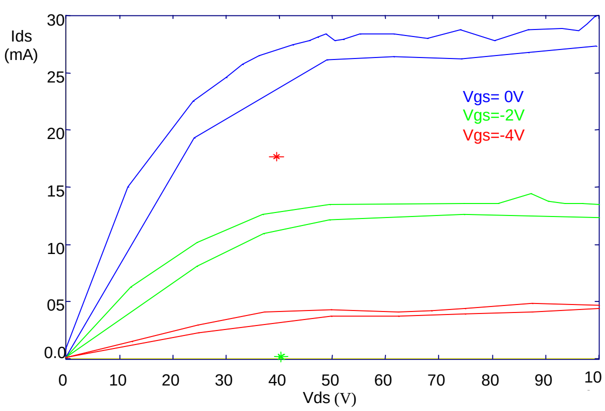

Fig-8 Measurement of the drain current for T=200°C and T=320°C

V. CONCLUSION

Trapping and thermal effects have been investigated for GaN MESFETs and it has been shown the trapping effects are predominant in the device tested. Those effects are mainly related to time constants associated to the electron capture and emission process. They are strongly affected either by light or by temperature. High temperature working of the MESFET has been demonstrated and characterized. Further work needs to be done in order to improve the material fabrication and it has been shown that pulsed measurements provide an invaluable tool to investigate various trapping and thermal effects.

ACKNOWLEDGEMENT

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